Abstract of the Disclosure

In a semiconductor memory device, a plurality of memory cell arrays, and each of them includes a plurality of memory cells in a matrix. A mode control unit outputs a delay control signal, and an instruction execution unit accesses to the plurality of memory cells based on an address and an address buffer control signal supplied externally. A command control unit outputs the address buffer control signal to the instruction execution unit based on a command supplied externally and the delay control signal. The command control unit outputs the address buffer signal in synchronization with a clock signal when the delay control signal is in an inactive state and the command is a write command or a read command in an ordinary operation mode. When the delay control signal is in an active state and the command is the write command in a write instruction delay operation mode, also when the delay control signal is in the active state and the command is the read command in a read instruction delay operation mode.